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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,716	10/22/2003	Nelson Gonzalez	19463-0002	3956

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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,716	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) *9-18 and 35-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,19-34 and 41-49* is/are rejected.

7)☒ Claim(s) *29,31 and 48* is/are objected to.

8)☒ Claim(s) *1-49* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-8, 29-34, and 41-49, drawn to a motherboard, classified in class 345, subclass 502.

   II. Claims 9-17, 24-28, and 35-38, drawn to coupling graphics controllers to a motherboard, classified in class 345, subclass 520.

   III. Claims 18-23 and 39-40, drawn to a computer, classified in class 345, subclass 501.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I, II, and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as a motherboard comprising a processor socket, a scalable interconnect, and video card slots. Invention II has separate utility such as coupling graphics controllers to a motherboard by providing a scalable interconnect, dividing the scalable interconnect into multiple high-speed connections, and routing the high speed connections to video slots. Invention III has separate utility such as a computer comprising a motherboard and multiple graphics controllers. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Ajit Vaidya on January 11, 2005 a provisional election was made without traverse to prosecute the invention of group I, claims 1-8, 29-34, and 41-49. Affirmation of this election must be made by applicant in replying to this Office action. Claims 9-28 and 35-40 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Specification

6. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract is 154 words in length and therefore exceed 150 words.

Claim Objections

7. Claim 29 is objected to because of the following informalities: Claim 29 recites "to the *to the* second video card slot" where it should recite "to the second video card slot". Appropriate correction is required.

8. Claim 31 is objected to because of the following informalities: Claim 31 recites "wherein the first video card slot and the first video card slot". Applicant is assumed to have meant "wherein the first video card slot and the *second* video card slot". Appropriate correction is required.

9. Claim 48 is objected to because of the following informalities: Claim 48 recites "the first and the second video slots video slots" where it should recite "the first and the second video slots". Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 31 and 48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 31 recites the limitation "the first video card slot". There is insufficient antecedent basis for this limitation in the claim.

Claim 48 recites the limitation "the central processing unit". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1-7, 29-34, and 41-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1) in view of Sauber (US 20040181617A1).

15. With regard to Claim 1, Levy describes a chipset (104, Figure 1) for managing data transfers within the computing device [0014]; a scalable interconnect (Device 0) connecting to the computing device [0021]; and a plurality of ports or high-speed video card slots [0016] connected to the interconnect [0021].

However, Levy does not teach that the computing device is a motherboard. However, Sauber describes a motherboard comprising a chipset (20, Figure 1) for managing data transfers within the motherboard [0005, 0011] and a scalable interconnect connecting to the motherboard [0009, 0011].

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Levy so that the computing device is a motherboard as suggested by Sauber. Motherboards are well-known in the art and widely used. Motherboards make it easy to add new features to the machine over time. Motherboards have opened the computer to creative opportunities for third-party vendors. The motherboard, by enabling

pluggable components, allows users to personalize a computer system depending on their applications and needs. The advantages of using a motherboard can be found in many publications, such as the howstuffworks website.

16. With regard to Claim 2, Levy describes a switch (116, Figure 3) connected to the interconnect (Device 0), wherein the switch distributes bandwidth from the interconnect to the plurality of high-speed video card slots [0021, 0017, 0018, 0016].

17. With regard to Claim 3, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a x16 connection, and wherein the switch (116, Figure 3) distributes bandwidth from the x16 connection to two x16 video card slots [0001, 0021, 0017, 0018, 0016].

18. With regard to Claim 4, Levy describes that the interconnect comprises at least a x32 connection [0001].

19. With regard to Claim 5, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect that is divided into two or more x16 connections between the chipset (104, Figure 1) and the plurality of high-speed video card slots [0001, 0014, 0016].

20. With regard to Claim 6, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising at least a x16 connection, and wherein the interconnect is divided into a x8 connection between the chipset and each of the plurality of high-speed video card slots [0001. 0016].

21. With regard to Claim 7, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a connection having at least 24 lanes, and wherein the interconnect is divided into a x8 connection between the chipset (104, Figure 1) and one of the plurality of high-speed video card slots and a x16 connection between the chipset and another of the plurality of high-speed video card slots [0001, 0016].

22. With regard to Claim 29, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses video card slots comprising a first video card slot and a second video card slot, the interconnect comprising a first x16 connection to the first video card slot and a second smaller-scaled connection to the second video card slot [0001, 0016].

23. With regard to Claim 30, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Levy gives an example wherein the second connection is a x4 connection. Therefore, Levy discloses a second connection that is at least one of a x1, x2, x4, and x8 connection [0001].

24. With regard to Claim 31, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Levy gives an example of a first video card slot and a second video card slot both having the prespecified dimensions of a x4 link. Therefore, Levy discloses a first video card slot and a second video card slot having first prespecified dimensions [0001, 0016].

25. With regard to Claim 32, Levy describes ports or a peripheral slot connected to the interconnect (Device 0, Figure 2). In Figure 2, the peripheral slot is shown to have the prespecified dimensions a x8 link, and the first dimensions are for a x4 link and a x8 link [0020]. Therefore, Levy discloses a peripheral slot having second prespecified dimensions, wherein the second dimensions differs from the first dimensions.

26. With regard to Claim 33, Levy describes that a graphics card can be coupled to any of the video card slots [0016, 0020]. Therefore, Levy discloses first dimensions of the video card slots that are selected to allow a graphics card to be coupled to any of the video card slots.

27. With regard to Claim 34, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses a graphics card that is designed to be used with a x16 connection [0001, 0016].

28. With regard to Claim 41, Levy describes a computing device for supporting multiple video cards, the computing device comprising a processor socket (104, Figure 1) adapted to receive a processor (102) [0014]; a scalable interconnect (Device 0) that provides data paths to the processor socket (Figure 1), wherein the scalable interconnect is selectively divided as needed to allocate the data paths [0016-0017]; and video card slots connected to the interconnect, wherein each of the video card slots is specifically adapted for coupling to a graphics card [0021, 0016].

However, Levy does not teach that the computing device is a motherboard and that the processor is a central processing unit (CPU). However, Sauber describes a motherboard comprising a chipset (20, Figure 1) for managing data transfers within the motherboard [0005, 0011] and a scalable interconnect connecting to the motherboard [0009, 0011], as discussed in the rejection for Claim 1. Sauber also describes a processor socket (20, Figure 1) adapted to receive a CPU (12) [0005].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Levy so that the processor is a CPU as suggested by Sauber. CPUs are well-known in the art and are widely used. The CPU is the brains of the computer. The CPU is needed to perform most of the calculations. In terms of computing power, the CPU is the most important element of a computer system. This can be found in many publications, such as the Webopedia Online Encyclopedia.

29. With regard to Claim 42, Levy gives the example of the video card slots all having the dimensions of a x4 link [0001]. Therefore, Levy discloses video card slots having substantially similar dimensions.

30. With regard to Claim 43, Levy describes that the multiple graphics cards can be any type of graphics cards [0016]. Therefore, Levy discloses that multiple similar graphics cards can be coupled to the computing device.

However, Levy does not teach that the computing device is a motherboard. However, Sauber describes a motherboard comprising a chipset (20, Figure 1) for managing data transfers within the motherboard [0005, 0011] and a scalable interconnect connecting to the motherboard [0009, 0011], as discussed in the rejection for Claim 1.

31. With regard to Claim 44, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy

discloses that each of the video card slots is configured to couple with a graphics card designed to be used with a x16 connection [0001, 0016].

32. With regard to Claim 45, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect (Device 0, Figure 1) comprising a first data path (Link 1) and a second data path (Link 2), each of the first and second data paths connecting the processor socket (104) to different video card slots, the first data path being equal to or larger in scale than the second path [0001, 0016].

33. With regard to Claim 46, Claim 46 is similar in scope to Claim 30, and therefore is rejected under the same rationale.

34. With regard to Claim 47, Claim 47 is similar in scope to Claim 32, and therefore is rejected under the same rationale.

35. With regard to Claim 48, Levy describes a high performance computer including a processor socket (104, Figure 1) adapted to receive the processor (102) [0014], a scalable interconnect (Device 0) that provides data paths to the processor (Figure 1), wherein the scalable interconnect is selectively divided as needed to allocate the data paths [0016-0017], and a first and a second video slots, wherein the first and the second video slots connect to one or more of

the data paths [0020], the first and the second video slots have a substantially similar physical configuration [0001], as discussed in the rejection for Claim 42, wherein the video slot physical configuration is selected to allow the first and the second video slots to accept a graphics card; and a first graphics card coupled to the first video slot [0016].

However, Levy does not teach that the computing device is a motherboard and that the processor is a central processing unit (CPU). However, Sauber describes a motherboard comprising a chipset (20, Figure 1) for managing data transfers within the motherboard [0005, 0011] and a scalable interconnect connecting to the motherboard [0009, 0011], as discussed in the rejection for Claim 1. Sauber also describes a processor socket (20, Figure 1) adapted to receive a CPU (12) [0005], as discussed in the rejection for Claim 41.

36. With regard to Claim 49, Levy describes that each video slot has a graphics card coupled to it [0016]. Therefore, Levy discloses a second graphics card coupled to the second video slot.

37. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1) in view of Sauber (US 20040181617A1), further in view of Grimaud (US005546530A).

Levy and Sauber are relied upon for the teachings as discussed above relative to Claim 1.

However, Levy and Sauber do not teach that a display area is divided into separate sections, one or more graphics processing units (GPUs) are dedicated to graphics processing related to each of the display sections; and the GPUs are connected to the high-speed video card slots. However, Grimaud describes that a display area is divided into separate sections, one or

more graphics processing units (GPUs) (100A, 100B, Figure 3; Col. 3, lines 55-62) are dedicated to graphics processing related to each of the display sections (Col. 2, lines 53-60); and the GPUs are connected to the high-speed video card slots (Col. 2, lines 41-44).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Levy and Sauber so that a display area is divided into separate sections, one or more graphics processing units (GPUs) are dedicated to graphics processing related to each of the display sections; and the GPUs are connected to the high-speed video card slots as suggested by Grimaud. Grimaud describes that as the complexity of the graphical scene increases, rendering images within acceptable animation limits becomes more difficult both in terms of the number of objects to be displayed and the time it takes for the graphics computers to render the image. Thus, a user with a limited graphics library or processing capability will be unable to create more intricate animated environments. By allowing animation information and processor power from a plurality of different sources to be combined, the apparatus is able to render complex graphical scene which one machine would be incapable of doing alone (Col. 2, lines 27-41).

Prior Art of Record

Gary Brown, "How Motherboards Work",
http://electronics.howstuffworks.com/motherboard.htm/printable.

"CPU", http://www.webopedia.com/TERM/C/CPU.html.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 703-305-4418. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Matthew C. Bella

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